UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,009	11/26/2003	Siva Ramakrishnan	ITL.1602US (P17216)	9554

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EXAMINER
BRADLEY, MATTHEW A

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/723,009	RAMAKRISHNAN, SIVA
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _10 July 2007_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1,3-23 and 25-29_ is/are pending in the application.

　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,3-23 and 25-29_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　a)☐ All b)☐ Some * c)☐ None of:

　　1.☐ Certified copies of the priority documents have been received.

　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
　Paper No(s)/Mail Date _2/6/06_.

4)☐ Interview Summary (PTO-413)
　Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 10 July 2007.

Applicant's arguments have been carefully and fully considered but are moot in view of

the new ground(s) of rejection as necessitated by amendment. Accordingly, this action

has been made FINAL.

Claim Status

Claims 1, 3-23, and 25-29 remain pending and are ready for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

Claims **1** and **3-21** are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention.

Claims **5-8** are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. As per dependent claim **5** line 6, the phrase, 'the

data being compressed' appears. This is indefinite, as there is no data that is presently

being compressed.

Claims **1** and **3-21** are rejected under 35 U.S.C. 112, second paragraph, as

being incomplete for omitting essential elements, such omission amounting to a gap

between the elements. See MPEP § 2172.01. The omitted elements are the device

within the apparatus that is assigning priority to the read operations.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1**, **3-4**, **9**, and **14-21** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Benveniste et al (U.S. 6,353,871), hereinafter referred to as

Benveniste, and in view of Harris (U.S. 6,601,151), hereinafter referred to as Harris.

As per independent claim **1**, Benveniste teach,

- o a compression cache to store a plurality of uncompressed data, wherein
     the compression cache is organized as a sectored cache that has
     associated tags that are on-die; (Figures 1 and 2 and as taught in Column
     3 lines 6-18, the compressed memory is divided into fixed-size sectors;
     the CPU subsystem as taught in Column 2 line 65 to Column 3 line 5,
     contains a TLB on-die that works with the MMU in referencing CTT
     entries, or tags)

- o a compressed memory to store a plurality of compressed data; and
     (Column 1 lines 44-47).

- o a compressed memory pointer table (CMPT) to store a plurality of pointers
     (Column1 line 54 to Column 2 line 11). *The Examiner is interpreting the*

directory structure of Benveniste to be the pointer table that stores a

plurality of pointers pointing to the data as instantly claimed. Each

directory entry in the directory structure maintains an address or pointer to

the respective data. Accordingly, the directory structure of Benveniste

anticipates the pointer table as instantly claimed.

Benveniste does not explicitly teach, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations.

Harris teaches, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations (Figure 4 as taught in Column 7 line 58 to Column 8 line 24).

Benveniste and Harris are analogous art because they are from the same field of endeavor namely, memory systems.

At the time of invention, it would have been obvious to one of ordinary skill in the art, having both the teachings of Benveniste and Harris before him/her to combine the memory read prioritization of Harris with Benveniste for the benefit of enhanced and improved performance.

The suggestion for doing so would have been that; processor performance can be enhanced by ascribing memory read requests higher priority than other requests (Column 7 line 58 to Column 8 line 24). Further, as further taught in the aforementioned citing of Harris, write requests are given the lowest priority. Thus, Harris obviates that which is instantly claimed in that the system assigns a higher priority to read operations in comparison to other operations.

Therefore, it would have been obvious to combine Benveniste with Harris for the memory read prioritization to obtain the invention as specified in claims 1, 3-4, 9, and 14-21.

As per dependent claim **3**, the combination of Benveniste and Harris teach, wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus (Column1 line 54 to Column 2 line 11 of Benveniste). *The Examiner notes that the individual directory entries anticipate the tags.*

As per dependent claim **4**, the combination of Benveniste and Harris teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 1 line 54-60 of Benveniste).

As per dependent claim **9**, the combination of Benveniste and Harris teach, wherein the CMPT is to store the plurality of pointers to the plurality of compressed data sequentially based on memory addresses for the plurality of compressed data (Column 5 lines 49-62 of Benveniste).

As per independent claim **14**, the combination of Benveniste and Harris teach,

- o receiving a memory address for the memory operation; (Column 3 line 13 of Benveniste)

- o storing a plurality of compressed data in a main memory; and (Column 3 lines 24-26 of Benveniste)

- o performing a tag match between the memory address and a first cache storing a plurality of tags for a compressed memory in the main memory (Column 3 lines 15-20 of Benveniste)

- o assigning a higher priority to compressed memory read operations in comparison to other operations (Figure 4 as taught in Column 7 line 58 to Column 8 line 24 of Harris).

As per dependent claim **15**, the combination of Benveniste and Harris teach, accessing a plurality uncompressed data access from a compression cache is if the tag match resulted in a hit (Column 3 lines 20-25 of Benveniste).

As per dependent claim **16**, the combination of Benveniste and Harris teach, locating a pointer and subsequently finding a compressed memory location based at least in part on the pointer if the tag match resulted in a miss for the memory operation for a read miss (Column 3 lines 10-30 of Benveniste).

As per dependent claim **17**, the combination of Benveniste and Harris teach, compressing the data and storing it in a compressed memory location for the memory operation for a write miss (Column 3 lines 10-30 of Benveniste).

As per independent claim **18**, the combination of Benveniste and Harris teach,

- o a processor; and (Column 1 lines 38-39 and Figure 1 item 102 of Benveniste) *The Examiner notes that a CPU as taught by Benveniste is a processor.*

- o a main memory, coupled to the processor, with a (Figure 1 item 108 of Benveniste).

- o a compression cache to store a plurality of uncompressed data; wherein the compression cache is organized as a sectored cache that has associated tags that are on-die (Figures 1 and 2 and as taught in Column 3 lines 6-18, the compressed memory is divided into fixed-size sectors; the CPU subsystem as taught in Column 2 line 65 to Column 3 line 5, contains a TLB on-die that works with the MMU in referencing CTT entries, or tags)

- o a compressed memory to store a plurality of compressed data; and (Column 1 lines 44-47 of Benveniste).

- o a compressed memory pointer table (CMPT) to store a plurality of pointers (Column1 line 54 to Column 2 line 11 of Benveniste). *The Examiner is interpreting the directory structure of Benveniste to be the pointer table that stores a plurality of pointers pointing to the data as instantly claimed. Each directory entry in the directory structure maintains an address or pointer to the respective data. Accordingly, the directory structure of Benveniste anticipates the pointer table as instantly claimed.*

- o And to assign a higher priority to compressed memory read operations in comparison to other operations (Figure 4 as taught in Column 7 line 58 to Column 8 line 24 of Harris).

As per dependent claim **19**, the combination of Benveniste and Harris teach, wherein the compression cache is a sectored cache (Item 266 of Figure 2 of Benveniste). *The Examiner notes that as discussed supra, the buffers of Benveniste*

anticipate the compression cache as instantly claimed. As shown in Figure 2, these

buffers are individual and thus sectored. Accordingly Benveniste anticipates the

compression cache as a sectored cache with the buffers.

As per dependent claim **20**, the combination of Benveniste and Harris teach,

wherein the compression cache has a plurality of associated tags that are incorporated

within a memory interface (Column1 line 54 to Column 2 line 11 of Benveniste). *The*

Examiner notes that the individual directory entries anticipate the tags.

As per dependent claim **21**, the combination of Benveniste and Harris teach,

wherein the plurality of pointers are to the plurality of compressed data based on a

plurality of cache block addresses (Column 1 line 54-60 of Benveniste).

Claims **5-7**, **10-12**, **22-23**, and **26-29** are rejected under 35 U.S.C. 103(a) as

being obvious over Benvensite in view of Harris and further in view of Van Doren et al

(U.S. 6,202,126) hereinafter referred to as Van Doren.

As per dependent claim **5**, the combination of Benveniste and Harris teach, a

CMPT offset calculator to provide an offset relative to the start of the CMPT based on

an actual address of the data being compressed (Column 6 lines 20-34 of Benveniste).

The combination of Benveniste and Harris does not teach, a victim buffer to store

at least one the entry that has been evicted from the compression cache.

Van Doren teach, a victim buffer to store at least one the entry that has been

evicted from the compression cache (Column 1 lines 10-12).

Benveniste and Harris and Van Doren are analogous art because they are from

the same field of endeavor, namely memory systems.

At the time of invention it would have been obvious to one of ordinary skill in the
art, having both the teachings of Benveniste and Harris, and Van Doren before him/her,
to integrate the victim buffers of Van Doren into the system of Benveniste and Harris so
displaced data from the cache has temporary storage.

The motivation for doing so would be that, "each CPU may also include victim
buffers for temporarily storing data which is displaced from its cache (Column 1 lines
10-12 of Van Doren)."

Therefore, it would have been obvious to combine Benveniste and Harris with
Van Doren to obtain the invention as specified in claims 5-7, 10-12, 22-24, and 26-29.

As per dependent claim **6**, the combination of Benveniste, Harris, and Van Doren
teach, wherein the memory interface is incorporated within a processor or a chipset
(Figure 2 of Benveniste). *The Examiner notes that item 260 of Figure 2 is shown as a*
part of the whole system. Accordingly, item 260 is part of a chipset.

As per dependent claim **7**, the combination of Benveniste, Harris, and Van Doren
teach, wherein the apparatus is incorporated within a memory controller hub (MCH) of
the chipset (Figure 3 item 260 of Benveniste).

As per independent claim **10**, Benveniste teach,

- o a first cache to store a plurality of tags for a compression cache; (Figure 3
  item 320)

- o an offset calculator to provide an offset relative to the start for a
  Compressed Memory Pointer Table (CMPT) based on an actual address
  of a data being compressed; and (Column 6 lines 20-34).

    o   a second cache to store a plurality of pointers for the CMPT (Figure 3 item

        330).

Van Doren teach,

    o   a victim buffer to store at least one the entry that has been evicted from

        the compression cache (Column 1 lines 10-12).

Harris teach,

    o   the apparatus to assign a higher priority to compressed memory read

        operations in comparison to other operations (Figure 4 as taught in

        Column 7 line 58 to Column 8 line 24 of Harris).

As per dependent claim **11**, the combination of Benveniste, Harris, and Van

Doren teach, wherein the memory interface is incorporated within a processor or a

chipset (Figure 2 of Benveniste). *The Examiner notes that item 260 of Figure 2 is*

shown as a part of the whole system. Accordingly, item 260 is part of a chipset.

As per dependent claim **12**, the combination of Benveniste, Harris, and Van

Doren teach, wherein the apparatus is incorporated within a memory controller hub

(MCH) of the chipset (Figure 3 item 260 of Benveniste).

As per independent claim **22**, Benveniste teach,

    o   a processor; and (Column 1 lines 38-39 and Figure 1 item 102) *The*

        Examiner notes that a CPU as taught by Benveniste is a processor.

    o   a memory interface, coupled to the processor, with a: (Figure 1 item 108).

    o   a first cache to store a plurality of tags for a compression cache; (Figure 3

        item 320)

- o   an offset calculator to provide an offset relative to the start for a

    Compressed Memory Pointer Table (CMPT) based on an actual address

    of a data being compressed; (Column 6 lines 20-34).

- o   and a second cache to store a plurality of pointers for the CMPT. (Figure 3

    item 330).

Van Doren teach,

- o   a victim buffer to store at least one the entry that has been evicted

    from the compression cache; (Column 1 lines 10-12).

As per dependent claim **23**, the combination of Benveniste, Harris, and Van

Doren teach, wherein the memory interface is incorporated within a processor or a

chipset (Figure 2 of Benveniste). *The Examiner notes that item 260 of Figure 2 is*

shown as a part of the whole system. Accordingly, item 260 is part of a chipset.

As per independent claim **26**, Benveniste teach,

- o   a processor, coupled to a memory bridge, the memory bridge to comprise;

    (Column 1 lines 38-39 and Figure 1 item 102) *The Examiner notes that a*

    CPU as taught by Benveniste is a processor.

- o   a first cache to store a plurality of tags for a compression cache; (Figure 3

    item 320)

- o   an offset calculator to provide an offset relative to the start for a

    Compressed Memory Pointer Table (CMPT) based on an actual address

    of a data being compressed; and (Column 6 lines 20-34).

- o a second cache to store a plurality of pointers for the CMPT and (Figure 3 item 330).

- o a main memory, coupled to the memory bridge, to comprise a (Figure 1 item 108).

- o compression cache to store a plurality of uncompressed data; (Column1 lines 52-52). *The Examiner is interpreting the buffers of Benveniste which store the uncompressed data to be the caches as instantly claimed.*

- o a compressed memory to store a plurality of compressed data; (Column 1 lines 44-47).

- o and a compressed memory pointer table (CMPT) to store a plurality of pointers (Column1 line 54 to Column 2 line 11). *The Examiner is interpreting the directory structure of Benveniste to be the pointer table that stores a plurality of pointers pointing to the data as instantly claimed. Each directory entry in the directory structure maintains an address or pointer to the respective data. Accordingly, the directory structure of Benveniste anticipates the pointer table as instantly claimed.*

Van Doren teach,

- o a victim buffer to store at least one the entry that has been evicted from the compression cache; (Column 1 lines 10-12).

As per dependent claim **27**, the combination of Benveniste, Harris, and Van Doren teach, wherein the compression cache is a sectored cache (Item 266 of Figure 2 of Benveniste). *The Examiner notes that as discussed supra, the buffers of Benveniste*

anticipate the compression cache as instantly claimed. As shown in Figure 2, these buffers are individual and thus sectored. Accordingly Benveniste anticipates the compression cache as a sectored cache with the buffers.

As per dependent claim **28**, the combination of Benveniste, Harris, and Van Doren teach, wherein the compression cache has a plurality of associated tags that are incorporated within the memory bridge (Column1 line 54 to Column 2 line 11 of Benveniste). *The Examiner notes that the individual directory entries as a whole anticipate the plurality of tags.*

As per dependent claim **29**, the combination of Benveniste, Harris, and Van Doren teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 1 line 54-60 of Benveniste).

Claims **8**, **13**, and **25** are rejected under 35 U.S.C. 103(a) as being obvious over Benvensite in view of Harris and further in view of Hasan (U.S. 6,044,416).

As per dependent claim **8**, the combination of Benveniste and Harris teach, the limitations as noted supra.

The combination of Benveniste and Harris does not teach, wherein the entry is evicted based on a first in first out (FIFO) protocol.

Hasan teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 1 lines 13-17).

Benveniste and Harris, and Hasan are analogous art because they are from the same field of endeavor, namely memory configuration.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Benveniste and Harris, and Hasan before him/her, to combine the FIFO protocol of Hasan into Benveniste and Harris for the benefit of a FIFO queue.

The suggestion for doing so is that Hasan shows that when FIFO is used, data that is received from an external input device is stored in sequential order and subsequently provided to the external output device in the same sequential order (Column 1 lines 13-17).

Therefore it would have been obvious to combine the FIFO interface of Hasan with Benveniste and Harris for the benefit of a FIFO queue to obtain the invention as specified in claims 8, 13, 25.

As per dependent claim **13**, Benveniste, Harris, and Hasan teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 1 lines 13-17 of Hasan).

As per dependent claim **25**, the combination of Benveniste, Harris, and Hasan teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 1 lines 13-17 of Hasan).

Response to Arguments

Applicant's arguments filed 10 July 2007 have been carefully and fully considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

With respect to Applicant's argument located within the fourth full paragraph of the first page of the remarks filed on 28 July 2006 (numbered as page 11) which recites:

"Applicant respectfully requests Examiner clearly show the Benveniste buffers are sectored and such that the associated tags are on-die."

The Examiner respectfully disagrees. As shown in Benveniste, Figures 1 and 2 and as taught in Column 3 lines 6-18, the compressed memory is divided into fixed-size sectors. Further, the CPU subsystem as taught in Column 2 line 65 to Column 3 line 5, contains a TLB on-die that works with the MMU in referencing CTT entries, or tags.

With respect to Applicant's argument located within the fourth full paragraph of the first page of the remarks filed on 28 July 2006 (numbered as page 11) which recites:

"Furthermore, in the Applicant's pending patent application, the apparatus assigns a higher priority to compressed memory read operations in comparison to other operations, such as, write accesses to compressed memory and other read operations. In contrast, the prior art does not assign a different priority to the different operations."

The Examiner respectfully disagrees and refers Applicant's the rejection made supra that addresses this new limitation in the claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any
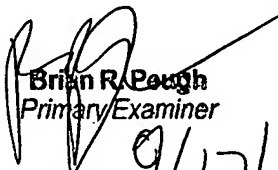
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Matthew Bradley whose telephone number is (571) 272-

8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BRP/mb

Brian R Peugh
Primary Examiner
9/17/07